REMARKS

Applicant respectfully requests that the Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this amendment presents claims in better form for consideration on appeal. Applicant submits that thus there is a good and sufficient reason why this amendment is necessary, why this amendment was not earlier presented, and why this amendment should be admitted now. Furthermore, applicant believes that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal.

The Examiner has noted the incorrect filing receipt given to this application.

The abstract of the specification is objected to because of minor informalities.

Claims 1-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy *et al.* ("Levy").

Claims 3, 4, and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy

Claims 1-14 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending application no. 09/023,170 and claims 1-17 of copending application no. 09/023,234.

Claims 1-14 are pending.

Claims 1-2, 4-11, and 13-14 have been amended. It is respectfully submitted that no new matter has been introduced by the amendments made herein.

Specification Objections

The Examiner has objected to the abstract of the disclosure because it is not clear what is meant by the phrase "system memory module." Accordingly, a new abstract has been provided to correct this informality. Thus, applicant requests the objection to the abstract be withdrawn.

35 U.S.C. § 102(b) Rejection

The Examiner has rejected claims 1-14 under 35 U.S.C. §102(b) as being anticipated by Levy. In particular, the Examiner states:

> Regarding claims 1, 12, and 13, Levy shows a memory module 30 which includes a memory module controller and a plurality of memory devices (low stack 0-3 and high stack 0-3) in Fig. 1.
>
> Levy shows the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42 and their input and output lines. Levy shows the claimed first interface circuitry (input lines into memory transceiver 41 and memory control and timing unit 42) which receives a first memory transaction from a system memory controller (memory management unit 22) in a first format as claimed.
>
> Levy further shows the claimed control logic (memory transceiver 41 and memory control and timing unit 42) which is coupled to the first interface circuitry and converts the first memory transaction into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory format is clearly different from the first memory transaction format since the outputs of the memory transceiver 41 and memory control and timing unit 42 are clearly different form their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

(p.4 Office Action 7/3/00).

Applicant respectfully submits that claim 1, as amended, is not anticipated by Levy. To anticipate claim 1, Levy must disclose each and every limitation of claim 1. Claim 1 includes the limitations of:

> A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:
>
> first interface circuitry to receive from the system memory controller a first memory transaction in a first format; and
>
> control logic coupled to the first interface circuitry and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

Levy, however, fails to disclose a memory module controller having a first interface circuitry and a control logic coupled to the first interface circuitry in the which the control logic is to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices as recited in claim 1. Levy further fails to disclose that the second format of the second memory transaction is different form the first format of the first memory transaction as recited in claim 1.

Levy, in Figure 1, discloses a memory module 30 coupled to associative memory 24. memory module 30 includes a memory transceiver 41 and memory control and timing circuit 42 coupled to low and high stacks 44 and 45, respectively. The Examiner associates memory transceiver 41 and memory control and timing circuit 42 of Levy with the claimed memory module controller as recited in claim 1.

The memory transceiver 41 and memory control and timing 42, however, are not related to converting or reformatting a memory transaction in a first format into a memory transaction in a second format. In particular, Levy discloses that:

> . . . During a writing operation, the associative memory 24 transmits BYTE MASK signals (FIG. 5) to the memory control and timing circuit 42 thereby to select one byte or some combination of bytes in the addressed location.

> Still referring to FIGS. 1 and 5, the associative memory 24 transmits an ADDRESS PARITY signal which is based upon the value of the address and various control signals that initiate a memory cycle and also data signals if data is being transferred from the associative memory 24. Next the associative memory 24 transmits a START signal that enables the memory control and timing circuit 42 (FIG. 1) to initiate a memory cycle. The circuit 42 transmits back to the associative memory 24 an ACKNOWLEDGE signal that terminates the address and control signals and the BYTE MASK, parity, data and START signals. During a reading memory cycle, the associative memory 24 can initiate another memory cycle with another memory until after the ACKNOWLEDGE signal is terminated.

(Levy Col. 8, lines 41-60).

Thus, Levy teaches that memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, Levy does not teach that the memory control and timing circuit 42 converts or reformats a first memory transaction into a second memory transaction.

Therefore, for the above reasons, claim 1 is not anticipated by Levy. Given that claims 2-11 depend directly or indirectly on claim 1, claims 2-11 are not anticipated by Levy.

Applicant respectfully submits that claim 12 is not anticipated by Levy. To anticipate claim 12, Levy must disclose each and every limitation of claim 12. Claim 12 includes the limitations of:

> A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:
>
> means for receiving from the system memory controller a first memory transaction in a first format; and
>
> means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

(Claim 12)(emphasis added).

Levy, however, fails to disclose a memory module controller having means for receiving from the system memory controller a first memory transaction in a first format and a means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction as recited in claim 12.

As noted above, Levy does not teach converting or reformatting of memory transactions by a memory module controller. Therefore for the above reasons, claim 12 is not anticipated by Levy.

Applicant respectfully submits that claim 13, as amended, is not anticipated by Levy. To anticipate claim 13, levy must disclose each and every limitation of claim 13. Claim13 includes the limitations of:

> A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module comprising:
> first interface circuitry to receive from the system memory controller a first memory transaction in a first format; and
> control logic coupled to the first interface circuitry and to reformat the first memory transaction such that the plurality of memory devices perform the reformatted first memory transaction.

(Claim 13)(emphasis added).

Levy, however, fails to disclose a memory module controller having a first interface circuitry to receive from the system memory controller a first memory transaction in a first format and a control logic coupled to the first interface circuitry and

to reformat the first memory transaction such that the plurality of memory devices perform the reformatted first memory transaction as recited in claim 13.

As noted above, Levy does not teach converting or reformatting of memory transactions by a memory module controller. Therefore for the above reasons, claim 13 is not anticipated by Levy. Given that claim 14 is dependent on claim 13, claim 14 is not anticipated by Levy.

Accordingly, applicant respectfully submits that claims 1-14 are not anticipated by Levy and are patentable over the cited art of record.

35 U.S.C. § 103(a) Rejection

The Examiner has rejected claims 3, 4, and 5 under 35 U.S.C. § 103(a) as being unpatentable over Levy. In particular, the Examiner states:

> Levy shows separate address, data, and command lines for between the system memory controller and the plurality of memory devices on the memory module. He does not teach that his transactions include time-multiplexed address, data, and command information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the information to save signal lines and their associated cost and space. Additionally, once the skilled artisan multiplexed information, he would have to provide the claimed request handling logic to demultiplex it to the control logic.

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It is respectfully submitted that the Examiner relies on impermissible hindsight to render claims 3, 4, and 5 obvious. Nowhere in Levy does it disclose or suggest a memory transaction including time multiplexed address and command information, a request handling logic to separate address and command information and to provide separate address and command information to the control logic, or the request handling logic to

separate the time multiplexed data information as claimed with respect to claims 3, 4, and 5.

Furthermore, because Levy fails to disclose the limitations of claim 1 and claims 3, 4, and 5 are dependent directly or indirectly on claim 1, claims 3, 4, and 5 are not obvious over Levy. Accordingly, applicant respectfully submits that claims 1-14 are not obvious over Levy and are patentable over the cited art of record.

Double Patenting Rejection

Claims 1-14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/023,170 and claims 1-17 of copending Application No. 09/023,234.

Upon a condition of allowance of one or more claims, applicant will submit a timely filed terminal disclaimer.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the above rejections and objections set forth in the Office Action mailed July 3, 2000 have been overcome. Accordingly, applicant respectfully request that claims 1-14 be found in a condition of allowance.

If a telephone interview will expedite the prosecution of the application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Sang Hui Michael Kim
Reg. No. 40,450

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300